ML4013

Technical Reference

MSA Compliant 100G

CFP Electrical Passive Loopback Module

multiLane

Table of Contents

ML4013 CFP 10x10G Passive Loopback Module | Key Features

- Passive CFP loopback module, 10 TX & 10 RX Lanes operating at 100 Gb/s per lane
- Programmable Power Dissipation up to 24 W, custom modules can go up to 40 W
- Custom Memory Maps
- RX_LOS-Alarm driven by TX_DIS control
- High performance Signal Integrity traces
- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI)
- 3 Status LED indicator
- Built with advanced PCB material
- Temperature sensing
- Insertion counter
- Cut-Off Temperature preventing module overheating
- Hot Pluggable module

LED Indicator

Green (Solid) - Signifies that the module is operating in high power mode.
Amber (Solid) - Signifies the module is operating in low power mode.
Green / Amber (Blinking) - Signifies that the module is overheated and the temperature high alarm is asserted.

Operating Conditions

Recommended Operating Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Case Temperature	T_C		0		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.60	V
Data Rate	Rb	Guaranteed to work at 32 Gbps per lane	0		100	Gbps
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		24	W

1. General Description

The ML4013 is a CFP passive electrical loopback module with a hot pluggable form factor designed for high speed testing applications for CFP host ports. The ML4013 is designed for 100 Gigabit Ethernet applications and provides 10x10G RX and TX lanes, a MDIO module management interface and all the CFP MSA hardware signals.

The ML4013 loops 10-lane of 10 Gb/s transmit data from the Host back to 10-lane of 100 GB/s receive data to the Host.

The ML4013 provides programmable power dissipation up to 24 W allowing the module to emulate all the CFP power classes.

2. Functional Description

2.1 Management Data Interface – MDIO

The ML4013 supports the MDIO interface specified in IEEE802.3 Clause 45.
A dedicated MDIO logic block in the CFP module to handle the high rate MDIO data and a CFP register space that is divided into two register groups, the Non-Volatile Registers (NVR) and the Volatile Registers (VR). The NVRs are connected to a Non-Volatile Memory device (NVM) for ID/Configuration data storage. Over the internal bus system, the VRs are connected to a device that executes the Host control commands and reports various Digital Diagnostic Monitoring (DDM) data. Please Note that in the rest of this document, independently of implementation, CFP registers are also referred as NVRs or VRs.

The ML4013 specifications are the following:

- Supports MDC rates up to 4 MHz.
- CFP Registers at MDIO Device Address 1 as specified by CFP MSA.
- Supports various Physical Addresses thus allowing communication with many modules plugged to the same Host with different Port Addresses (PRT_ADDR0-4) assigned.

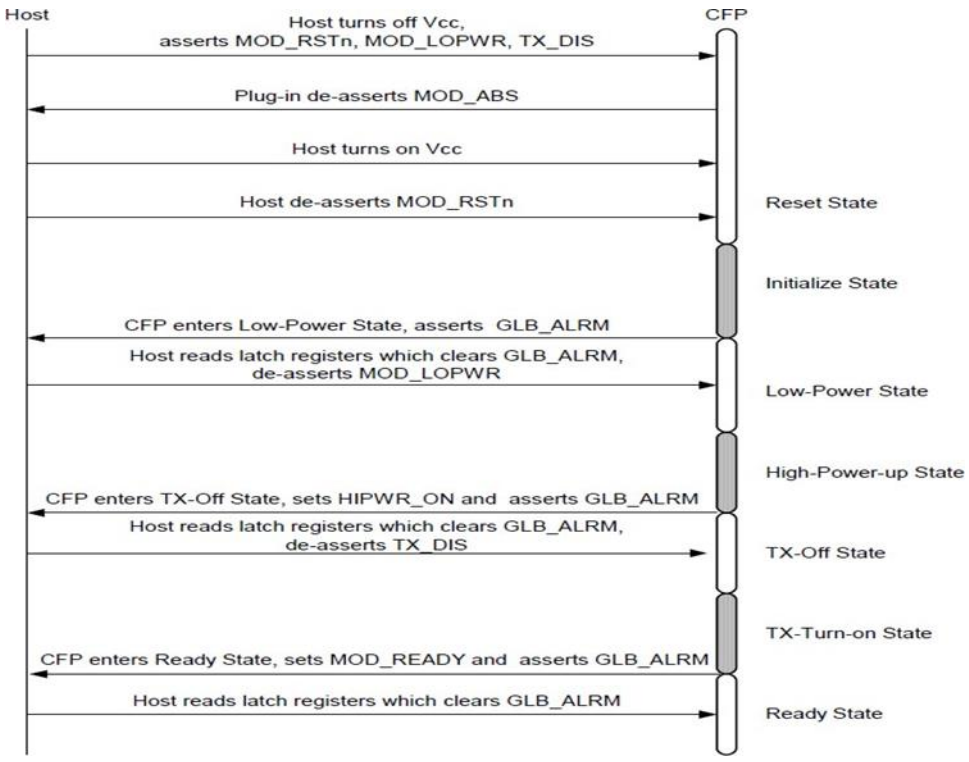
CFP registers use fast memory to shadow the NVM data and the DDM data. The shadow registers decouple the Host-side timing requirements from the module's internal processing, timing, and hardware control circuit introduced latency.

CFP shadow register set meets the following requirements:

- It supports dual access from the Host and from module internal operations such as NVM and DDM data transfers.
- It supports continuous Host access (read and write) with fast access memory at maximum MDC rates of 4 MHz.
- It allows the uploading of NVM content into the CFP shadow register during module initialization. Data saving from CFP shadow register to NVM is supported.
- It supports the DDM data update periodically during the whole operation of the module. The maximum data refresh period is 1 ms (real time temperature monitoring).
- It supports the whole CFP register set including all NVRs and VRs.
- Incomplete or otherwise corrupted MDIO bus transactions are purged from memory and disregarded.
- The port address is allowed to change on the fly without a module reset.

2.2 Initialization Sequence

The Startup sequence for the ML4013 is defined below:



MOD_RSTs assertion drives the CFP module to a reset state, at this stage the MDIO interface will be held in a high impedance state, the Host will read 'FFFF'h from any address, while host write operations will have no effect.

Upon the de-assertion of MOD_RSTs, the CFP module exists to an initialize state which is a transient state.

The Initialization time required is less than 1 second. When Initialization state is completed, the CFP module will enter a Low-Power state; at this point MDIO becomes available for R/W operations.

2.3 GLB_ALRM

Below is the flowchart for GLB_ALRM signal during CFP states transitions:

Figure 1: Flowchart for GLB_ALRM Signal

GLB _ALRM is de-asserted during Reset and Initialize state, it is asserted in Low-Power, High- Power-up, TX-Off and TX-Turn-on states, then de-asserted again when Ready state is reached. GLB_ALRMn is the hardware pin, and is the inverse of GLB_ALRM.

The below example can be run in order to check for correct module initialization and GLB_ALRM signal:

- Assert MOD_LOPWR and TX_DIS, Deassert MOD_RSTn: GLB_ALRMn should be HIGH (module in Reset state)
- Assert MOD_RSTn (module exits Reset state into Low Power state): GLB_ALRMn should be LOW
- Deassert MOD_LOPWR (module exits Low Power into TX-Off state): GLB_ALRMn should stay LOW
- Deassert TX_DIS (module enters Ready state): GLB_ALRMn should go HIGH

2.4 MDIO Signals, Addressing and Frame Structure

2.4.1 Port Address (PRTADR):

As per the port address used, the module will work on any MDIO Physical port address which can be set by the HW input signals PRTADR [4:0]. So when using 2 or more CFP slots, each of them can be configured to a different Port Address.

PRTADR0	MDIO Physical Port address bit 0
PRTADR1	MDIO Physical Port address bit 1
PRTADR2	MDIO Physical Port address bit 2
PRTADR3	MDIO Physical Port address bit 3
PRTADR4	MDIO Physical Port address bit 4

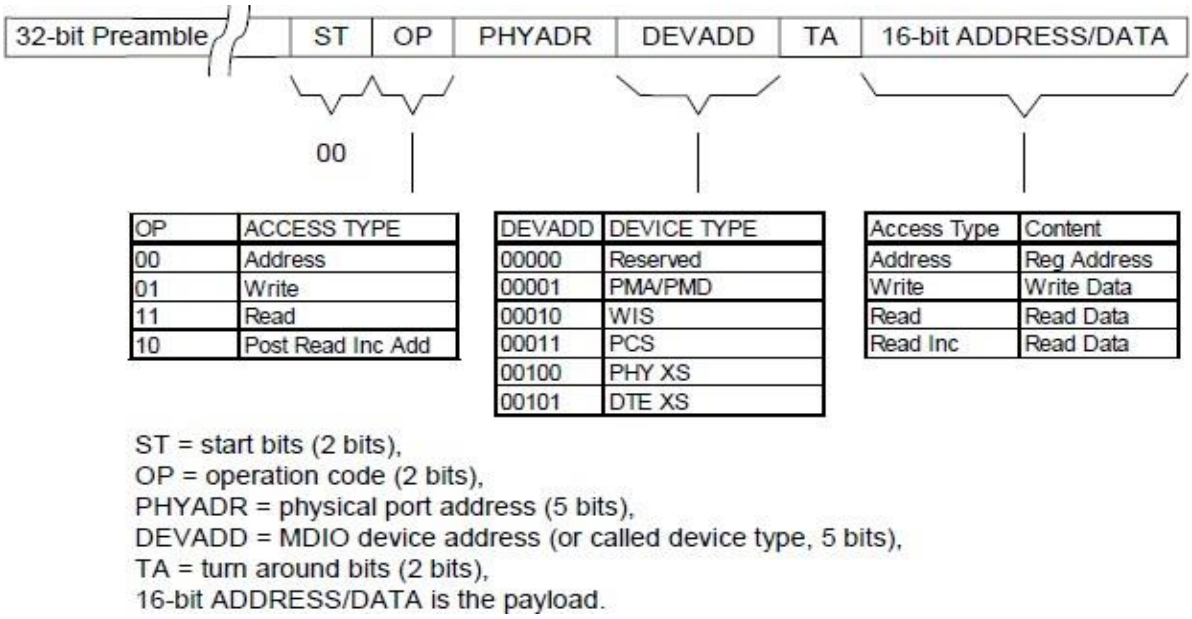
Figure 2: Port Address (PRTADR)

2.4.2 Device Address (DEVADD):

MDIO Device Address consists of 5 bits that are sent in MDIO frames, CFP MSA specifies that CFP register Set should be addressed using Device Address = 1, Thus CFP register space is available in the ML4013 on D.A=1.

2.4.3 MDIO Frame:

The Below Frame shows all segments of an MDIO Packet, PHYADR are the 5 bits Physical Address and DEVADD are the 5 bits Device Address.



OP	ACCESS TYPE
00	Address
01	Write
11	Read
10	Post Read Inc Add

DEVADD	DEVICE TYPE
00000	Reserved
00001	PMA/PMD
00010	WIS
00011	PCS
00100	PHY XS
00101	DTE XS

Access Type	Content
Address	Reg Address
Write	Write Data
Read	Read Data
Read Inc	Read Data

ST = start bits (2 bits),
OP = operation code (2 bits),
PHYADR = physical port address (5 bits),
DEVADD = MDIO device address (or called device type, 5 bits),
TA = turn around bits (2 bits),
16-bit ADDRESS/DATA is the payload.

Figure 3: MDIO Frame

2.5 CFP Register Set

All registers are supported in memory map (Refer to table below), the set of registers starting from 0x8000 to 0x9F00 are implemented as NVR registers, and these registers are always read from NVM during initialization and mapped to corresponding addresses.
All VR (Volatile Registers) are set to zero or to MSA defaults value upon module initialization.
The NVR values are saved to NVM by calling the SAVE NVR function. The base ID registers are initially set, but the user can change them if required.

CFP Register Allocation					
Starting Address In Hex	Ending Address In Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Received for IEEE 802.3 use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID registers.
8080	80FF	RO	128	8	CFP NVR 2. Extended ID registers.
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers.
8180	81FF	RO	128	8	CFP NVR 4.
8200	83FF	RO	4x128	N/A	MSA Reserved.
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers.
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers.
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA.
8800	887F	R/W	128	8	User NVR 1. User data registers.
8880	88FF	R/W	128	8	User NVR 2. User data registers.
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA.
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use.
9000	9FFF	RO	4096	N/A	Reserved for vendor private use.
A000	A07F	R/W	128	16	CFP Module VR 1. CFP Module level control and DDM registers
A080	A0FF	RO	128	16	Reserved by CFP MSA.
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA.
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific registers.
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific registers.
A300	A3FF	RO	2x128	N/A	Reserved by CFP MSA.
A400	A47F	R/W	128	16	Host Lane VR 1. Host lane specific registers.
A480	AFFF	RO	23x128	N/A	Reserved by CFP MSA.

3. ML4013 specific features

3.1 User NVR Restore and Save Function (0xA004)

To write permanently to User NVR registers (0x8000→ 0x9F00) the Host shall use the "Save" function to store the shadowed NVR data into underlying NVM. The host only needs to perform a single Save operation to copy the entire User NVR shadow registers to the underlying NVM after finishing editing the data.
Upon power-up or reset the User NVR shadow registers are "Restored" with NVM values. Note that the Restore function will overwrite the NVR shadow registers, losing any host-written values in them that have occurred since the last Save to the underlying NVM.
The NVR Access Control Register (A004h) provides the Save function for Host to save the User NVRs content.
Bit 5 in NVR Access Control Register is designated for User NVR save command.

A "1" written to bit 5 in register A004h initiates a User NVR Save.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
A004	1			**NVR Access Control**		0000h
		WO	5	User Restore and Save command	1: Save the user NVR section	0

So to call the user NVR save command user can write 0x0020 into register 0xA004.
The Save NVR duration is around 2 seconds. When this function is called it should be followed by a 2 second time wait.
During this process user the user can't write or read CFP registers.

3.2 PRG_ALRMs

The signals HIPWR_ON, MOD_READY, and MOD_FAULT are CFP internally generated signals and are defaults of the programmable alarm pins PRG_ALRMx.

The Following Table lists the corresponding functions for each of the PRG_ALRMs.

NAME	ALARM SOURCE	VALUE
HIPWR_ON	Module high-power-on indicator. PRG_ALRM1 MSA default.	0: Module not high powered up 1: Module high power up completed
MOD_READY	MOD_READY, module startup sequence done, PRG_ALRM2 MSA default.	0: Not done 1: Done
MOD_FAULT	Fault detected. PRG_ALRM3 MSA default.	0: No Fault 1: Fault

For testing purposes, PRG_ALRM3 can be manually controlled via bit 0 of register 0x9005.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9005	1			**PRG_ALRM control register**		0000h
		RW	0	PRG_ALRM3	0: De-assert PRG_ALRM3 pin 1: Assert PRG_ALRM3 pin	0

3.3 Temperature Monitor

The alarms and warnings of the CFP Loop Back are listed in the table 2, 3, and 4. Alarms are set in register 0x A01F in bits 8, 9, 10 and 11, and are continuously asserted and de-asserted when the corresponding alarms/warnings occur. addresses 0x8080, 0x8082, 0x 8084, and 0x 8086 are reference registers for temperature and alarms, they contain the default values (HA:75, HW:65, LA:0 and LW:5) and can be changed when desired. The module is continuously reading the temperature and storing its value in Register 0x A02F.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	LSB Unit
8080	2	RO	7~0	Temp High Alarm Threshold	These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125°C." MSB stored at low address, LSB stored at high address.	1/256 Deg C
8082	2	RO	7~0	Temp High Warning Threshold		
8084	2	RO	7~0	Temp Low Warning Threshold		
8086	2	RO	7~0	Temp Low Alarm Threshold		

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
A01F	1	RO		**Module Alarms and Warnings 1**		0000h
			11	Mod Temp High Alarm	Mod temp high Alarm 0: Normal, 1: Asserted	0
			10	Mod Temp High Warning	Mod temp high Warning 0: Normal, 1: Asserted	0
			9	Mod Temp Low Warning	Mod temp Low Warning 0: Normal, 1: Asserted	0
			8	Mod Temp Low Alarm	Mod temp Low Alarm 0: Normal, 1: Asserted	0

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
A02F	1	RO		Module Temp Monitor A/D Value	Measured case temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 deg C. MSA valid range is between – 40 and +125°C. Accuracy shall be better than +/- 3 deg C over the whole temperature range.	0000h

3.4 Insertion Counter

The Insertion counter contains the number of times the module was plugged in to a host. The insertion counter is incremented every time the module enters an initializing sequence, as it is nonvolatile it is always saved, and can be read anytime from register 0x9000.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	LSB Unit
9000	1			**Insertion Counter**		
		RO	0~7	Insertion Counter	Number of times the modules was plugged in a host	1 insertion

3.5 Programmable Power Dissipation & Thermal Emulation

Registers 0x9001 and 0x9002 are used for PWM control over MDIO. Are 8 bit data registers.
The consumed power changes accordingly when the value in this register is changed (only when in high power mode). In Low power mode the module automatically turns off PWM.
The values written in this register can be stored by calling the Save NVR function, thus the user can permanently change the initial power consumed in high power mode when the module is powered up by setting the register value and calling the Save NVR function. The PWM can also be used for module thermal emulation.
The module contains a thermal spot positioned where the optical transceivers usually are in an optical module that is heated relative to the related PWM register. It is programmed to 0 W by default, and can reach a maximum power of 24 W, with custom modules that can reach 40 W.
The module has three independent power spots of 8 W each. Two of them have static control and can be set to either 0 or 8 W. However, the third spot is dynamic, controlled by a PWM and can be programmed to any value between 0-8 W with a 32 mW precision.
Note that the led starts blinking when the temperature high alarm is reached.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9001	1	RW	0~7	PWM	0x00 to 0xFF that allows 0 to 8 W power consumption	0x00
9002	1	RW	0	Static power enable	Register bit to control 8 W power spot 1 1: Enable 0: Disable	0x00
			1		Register bit to control 8 W power spot 2 1: Enable 0: Disable	

3.6 RX_LOS

In the ML4013, RX_LOS is connected to TX_DIS, so RX_LOS output is driven by TX_DIS control, this does not report the actual LOS status of the module since the loopback is passive, but can be used for testing the CFP port pins on the host side.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9004	1			**Custom Alarms**		0000h
		RW	0	Prog RX_LOS	0: RX_LOS default operation (RX_LOS= TX_DIS) 1: Programmable RX_LOS (driven as per Soft RX_LOS bit)	0
		RW	1	Soft RX_LOS	0: RX_LOS HW signal set to LOW 1: RX_LOS HW signal set to High	0

3.7 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is defined in Register 0x9003. The module is continuously monitoring the temperature and checking its value against the Cut- Off temperature. A Temperature Cut-Off register is defined at address 0x9003. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the module gets 5 degrees below cut-off value of the temperature, the PWM goes back to its previous value.

The Maximum allowed Cut-Off temperature for the ML4013 is 90 deg C, so even if the value stored in register 0x9003 is higher than 90 the module will still Cut-Off power at 90 deg C, in case the value stored in 0x9003 is lower than 90 then it will be adopted instead of the default value.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Default Value
9003	1			Temp Cut-Off		
		RW	0~7	Cut-Off Value	0x00 to 0x5A (0 to 90 deg C)	0x55

3.8 Module Control and Status Registers

The below registers are implemented, and can be checked for module State and Control.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
A010	1			**Module General Control**		0000h
		RO	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert	0
		RW	13	Soft TX_Disable	Register bit for TX Disable function. 1: Assert	0
		RO	12-10	Reserved		0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert	0
		RO	8-6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD_LOPWR Pin	Logical state of the MOD_LOPWR pin. 1: Assert.	0
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin	0
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin	0
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin	0
		RO	0	Reserved		0

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
A016	1			**Module State**		0000h
		RO	15~9	Reserved		0
			8	High-Power-down	1: Corresponding state is active. Word value = 0100h.	0
			7	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.	0
			6	Fault State	1: Corresponding state is active. Word value = 0040h.	0
			5	Ready State	1: Corresponding state is active. Word value = 0020h.	0
			4	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.	0
			3	TX-Off State	1: Corresponding state is active. Word value = 0008h.	0
			2	High-Power-up State	1: Corresponding state is active. Word value = 0004h.	0
			1	Low-Power State	1: Corresponding state is active. Word value = 0002h.	0
			0	Initialize State	1: Corresponding state is active. Word value = 0001h.	0

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
A01D	1			**Module General Status**		
		RO	1	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable. 0: Module is not in high power on status. 1: Module is in high powered on status.	0

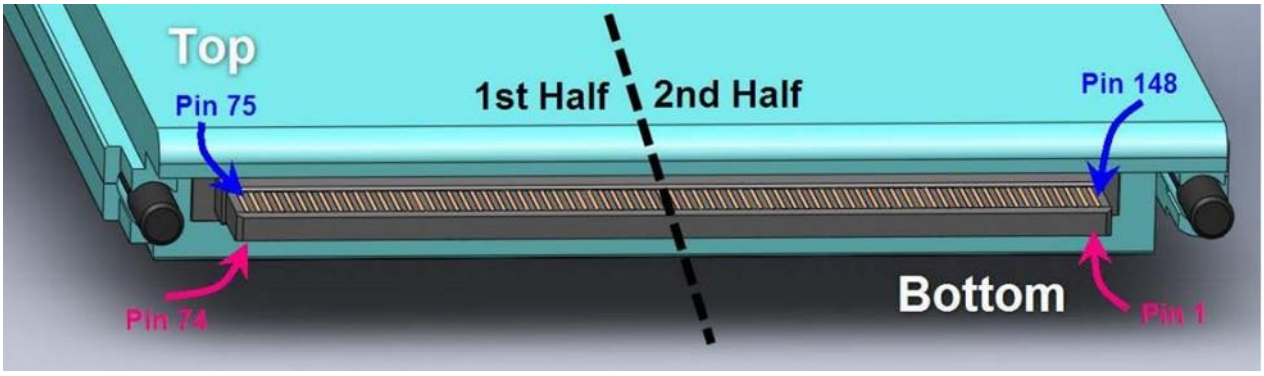
4. CFP-ACO Pin Allocation

4.1 Pin map

CFP pin mapping listed in CFP-MSA-HW-Spec-rev1.40 (table 5-6) is adopted for the ML4013.

Pins 21, 22, 27, 28 and 29 corresponding to VND_IO pins are used for the SWD programming interface. The host shall have these not connected or leave them tri-stated during module operation.

In case these are connected within the host, then the only requirement is for VND_IO_E (pin 29) to be left high during module operation, since driving it low will cause a hard reset of the module.



Bottom row (2nd half) pin description				
Position	**Symbol**	**I/O**	**Logic**	**Description**
1-5	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
6-15	3.3V			3.3V Module Supply Voltage
16-20	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
21	VND_IO_A	I/O		Module Vendor I/O A. Do not connect
22	VND_IO_B	I/O		Module Vendor I/O B. Do not connect
23	GND			
24	(TX_MCLKn)	O	CML	For optical waveform testing
25	(TXMCLKp)	O	CML	For optical waveform testing
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O C. Do not connect
28	VND_IO_D	I/O		Module Vendor I/O D. Do not connect
29	VND_IO_E	I/O		Module Vendor I/O E. Do not connect
30	PRG_CNTL1	I	LVCMOS w/PUR	Programmable control 1 set over MDIO, MSA default: TRXIC_RSTn, Tx and Rx ICs reset, “0”: reset, “1” or NC: enabled = not used
31	PRG_CNTL2	I	LVCMOS w/PUR	Programmable control 2 set over MDIO, MSA default: Hardware interlock LSB, “00” <8W, “01”<16W, “10”<24W, “11” or NC<32W = not used
32	PRG_CNTL3	I	LVCMOS w/PUR	Programmable control 3 set over MDIO, MSA default: Hardware interlock MSB, “00”<8W, “01”<16W, “10”<24W, “11” or NC<32W = not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set overMDIO, MSA default: HIPWR_ON, “1”: module power up completed, “0”: module not high powered up
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set overMDIO, MSA default: MOD_READY, “1”: Ready, “0”: not Ready

35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA default: MOD_FAULT, fault detected, “1”:Fault, “0”: No Fault
36	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes,”1” or NC = =transmitter disabled, “0”: transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/PUR	Module Low power mode “1” or NC: module in low power(safe) mode, “0”: Power-on enabled
Bottom row (1st half) pin description				
Position	**Symbol**	**I/O**	**Logic**	**Description**
38	MOD_ABS	O	GND	Module Absent. “1” or NC : module absent, “0”:module present, Pull up resistor on host
39	MOD_RSTn	I	LVCMOS w/PUR	Module Reset. “0” resets the module, “1” or NC: module enabled , Pull down resistor in module
40	RX_LOS	O	LVCMOS	Receiver loss of optical signal, “1”: low optical signal, “0” : normal condition
41	GLB_ALRMn	O	LVCMOS	Global alarm. “0”:alarm condition in any MDIO alarm register, “1”: no alarm condition, Open drain, Pull up resistor on host
42	PRTADR4	I	1.2V CMOS	MDIO Physical port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO Physical port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO Physical port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO Physical port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO Physical port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3 ae and ba)
48	MDC	I	1.2V CMOS	Management data clock (electrical specs as per 802.3 ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O F. Do not connect
51	VND_IO_G	I/O		Module Vendor I/O G. Do not connect
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O H. Do not connect
54	VND_IO_J	I/O		Module Vendor I/O J. Do not connect
55-59	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
60-69	3.3V			3.3V Module Supply Voltage
70-74	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
Top row (1st half) pin description				
Position	**Symbol**	**I/O**	**Logic**	**Description**
75	GND			
76	(RX_MCLKp)	I		
77	(RX_MCLKn)	I		

78	GND			
79	RX0p	I		
80	RX0n	I		
81	GND			
82	RX1p	I		
83	RX1n	I		
84	GND			
85	RX2p	I		
86	RX2n	I		
87	GND			
88	RX3p	I		
89	RX3n	I		
90	GND			
91	RX4p	I		
92	RX4n	I		
93	GND			
94	RX5p	I		
95	RX5n	I		
96	GND			
97	RX6p	I		
98	RX6n	I		
99	GND			
100	RX7p	I		
101	RX7n	I		
102	GND			
103	RX8p	I		
104	RX8n	I		
105	GND			
106	RX9p	I		
107	RX9n	I		
108	GND			
109	N.C			
110	N.C			
111	GND			

Top row (2nd half) pin description				
Position	**Symbol**	**I/O**	**Logic**	**Description**
112	GND			
113	TX0p	O		

114	TX0n	O		
115	GND			
116	TX1p	O		
117	TX1n	O		
118	GND			
119	TX2p	O		
120	TX2n	O		
121	GND			
122	TX3p	O		
123	TX3n	O		
124	GND			
125	TX4p	O		
126	TX4n	O		
127	GND			
128	TX5p	O		
129	TX5n	O		
130	GND			
131	TX6p	O		
132	TX6n	O		
133	GND			
134	TX7p	O		
135	TX7n	O		
136	GND			
137	TX8p	O		
138	TX8n	O		
139	GND			
140	TX9p	O		
141	TX9n	O		
142	GND			
143	N.C			
144	N.C			
145	GND			
146	REFCLKp			
147	REFCLKn			
148	GND			

5. High Speed Signals

High speed signals are electrically looped back from the TX side to the RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified by CFP MSA HW specs.

The Passive traces connecting TX to RX pairs are designed to support a data rate up to 10 Gbps.

Revision History

Revision number	Date	Description
0.1	04/28/2015	▪ Preliminary revision
0.2	05/04/2015	▪ Corrected table format of parag. 3.5
0.2.2	09/24/2020	▪ Format adjustments

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